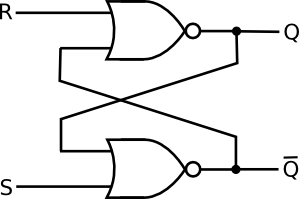
1. Given the SR latch pictured below, what is the state of Q and !Q when:







* 1. Q=1, Q!=0. With R=0 and S=0. THEN, R=1 and S=0.

Q: \_\_\_\_\_ !Q: \_\_\_\_\_



b. THEN, R=0 and S=1.

Q: \_\_\_\_\_ !Q: \_\_\_\_\_



c. THEN, R=0 and S=0.



Q: \_\_\_\_\_ !Q: \_\_\_\_\_



d. THEN, R=1 and S=0.



Q: \_\_\_\_\_ !Q: \_\_\_\_\_



e. THEN, R=1 and S=1.



Q: \_\_\_\_\_ !Q: \_\_\_\_\_



f. Describe the behavior of the SR latch and fill out the following truth table.

|  |  |  |  |
| --- | --- | --- | --- |
| S | R | Q | !Q |
| 0 | 0 | Q | !Q |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |

SET: Q “set” to 1

RESET: Q “reset” to 0

Both: Undefined

Neither: stays same

|  |  |  |
| --- | --- | --- |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |

SET: Q “set” to 1

Reset: Q “reset” to 0

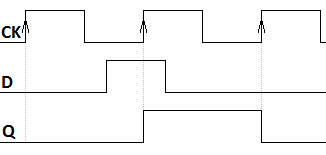
Both: Undefined

Neither: stays same

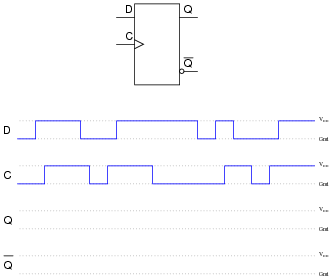
|  |  |  |
| --- | --- | --- |
| **S** | **R** | **Q** |
| 0 | 0 | Same |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | X |

1. A D-type flip-flop is a device in which the output presented at the DATA (D) pin will UPDATE the data being reflected on the OUTPUT (Q) pin on the EDGE of a clock signal.

Shown below is a *timing diagram* for a D-type flip flop. Fill out the missing lines (Q and !Q) on the **second** timing diagram below. C refers to the clock. This is a RISING EDGE triggered device.









1. Fill out the truth table below for a **rising-edge**-triggered D-type flip-flop.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| D | CK | Q | !Q | New Q | New !Q | Notes |
| 1 | 1 | 1 | 0 | 1 | 0 | Starting value |
| 1 | 1->0 | 1 | 0 | 1 | 0 | Clock is on FALLING EDGE |
| 0 | 0 | 1 | 0 | 1 | 0 |  |
| 0 | 0-1 | 1 | 0 | 0 | 1 | Clock is on RISING EDGE |
| 0 | 1 | 0 | 1 | 0 | 1 |  |

1. The D-type flip-flops supplied to you in your kits are CD4013s, which have SET and RESET lines. Those two inputs operate asynchronously. If there is a HIGH on the SET line, Q will immediately change to 1, regardless of the clock. Likewise, if there is a HIGH on the RESET line, Q will immediately change to 0, regardless of the clock. With that knowledge, fill out the truth table below (S=SET, R=RESET).

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| S | R | D | CK | Q | !Q | New Q | New !Q | Notes |
| 0 | 1 | 1 | 0 | X | X | 0 | 1 | High on RESET |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | High on SET |
| 0 | 0 | 1 | 0->1 (RISING EDGE) | 1 | 0 | 1 | 0 | Rising edge |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |  |